The demand for smaller and easily installable high-speed image sensors is increasing all the time: for fast scanning, industrial image processing and inspection systems, right through to traffic monitoring and automotive safety engineering, where the success of their development can ultimately be verified with highly-dynamic crash tests. For this kind of use, the customary systems, whose image sensors only deliver analog output signals and which have no internal sequence control, are not ideal, especially from a cost point of view. Instead, the key component for building such a high-speed data-acquisition system is a fast area sensor, which combines high data throughout with high light sensitivity. These two – basically contradictory – characteristics determine the performance limits of the overall system and must therefore be carefully balanced out to permit the widest possible range of applications: A high throughput is only possible with a short integration time of the incoming light and a short readout time. But this short integration time requires high quantum efficiency of the light-absorbing structure and a high conversion gain, because the amount of incoming light – especially with the minute pixel surfaces of high-resolution image sensors – is very small. So while the integration time can be reduced predominantly by physical means, a short readout time can be achieved with suitable structures, for example a high number of parallel readout paths.

If we look at a modern high-speed sensor (›Lupa 3000‹) with 2.9 MP and a frame rate of 485 fps (equivalent to approximately 1.4 GP/s), with integrated analog/digital converters (ADCs), a total of 32 differential LVDS (Low Voltage Differential Signaling) output channels and an integrated sequencer with built-in test function, immediately there is the question of the power loss. This should be as low as possible to prevent performance degradation due to self-heating. In the

<table>
<thead>
<tr>
<th>Operating mode</th>
<th>Speed</th>
<th>Compensation of</th>
</tr>
</thead>
<tbody>
<tr>
<td>Correlated double sampling in rolling shutter mode</td>
<td>High</td>
<td>Yes Yes</td>
</tr>
<tr>
<td>Double sampling in snapshot shutter mode</td>
<td>High</td>
<td>Yes No</td>
</tr>
<tr>
<td>Pipelined snapshot shutter mode</td>
<td>Highest</td>
<td>No No</td>
</tr>
</tbody>
</table>

A The three operating modes of 6T pixels
present case, the level is a moderate 1.1 W, which can still be dissipated without elaborate cooling methods.

**Sensor architecture as a complete subsystem**

The block diagram of a similarly constructed 1.3 MP high-speed CMOS image sensor (Lupa 1300-2) in Figure 1 shows all features of an autonomous system which communicates with its environment via a 10 Mbit/s bidirectional interface for control signals and status messages and has LVDS input and output clock signals and a synchronization channel.

In this case, the image data from the sensor array (image core 1280 x 1024) controls a total of 12 ADCs via the analog front end, which output their 10-bit output words likewise via 12 download channels with a data rate of 480 megasamples per second. The LVDS interface used for this seems to be emerging as the interface of choice for image sensors, since it allows very high data rates with a limited number of pins.

All required clock, control and bias signals are generated on-chip, by dividing the external high basic clock rate or generating from an integrated bandgap reference. An on-chip sequencer generates all the required control signals for the

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1 Complete CMOS imaging unit facilitates camera construction
The pixels of both high-speed image sensors with an N-well photo diode and a storage capacitor are laid out as in Figure 2, whereby the capacitor holds the photo diode signal for readout at a later stage. This type of pixel can support three operating modes: correlated double sampling in rolling shutter mode, double sampling in snapshot shutter mode, and pipelined snapshot shutter mode (see the INFO box and Table A).

**Parallel A/D conversion and fast, secure link**

The integration of part of the evaluation circuit on the one hand simplifies camera development but, on the other, limits their universal application considerably. These circuits include the analog/digital conversion with suitable digital output levels and measures for error detection during transfer.

In the sensors examined here (Figure 3), whose characteristic values are shown in Table B, multiple pipelined ADCs generate multiple digital output signals. They use fully differential circuits to improve their performance and noise immunity. A redundant signed digit (RSD) architecture and the digital error correction ensure low differential non-linearity (DNL), even if the comparators do not match exactly. The ADC gain errors and their offsets are reduced by appropriate circuits and auto-zeroing. In multiplex operation, their output data is then output via high-speed serial links in double data rate (DDR) mode.

Synchronization between the sensor and the surrounding host system, e.g. a high-speed camera, requires a suitable communication channel. This can either be done by sending control and status information via existing data channels using a standard procedure such as 8B/10B, or by adding separate channels. Because high-speed CMOS image sensors should provide the highest possible output-data rate and multiple output channels (here 12 or 32) have been set up for this, the first alternative is less suitable, because it reduces the speed of the sensor by 25 percent. Therefore two additional channels are provided for the output clock and the synchronization data.

Provision of the output clock dispenses with the need for clock recovery from the data signals. However, with the high transfer speed, it should be ensured that each channel has skew correction to balance out, for example, different runtimes.

### Table B: Characteristic values of the high-resolution image sensors

<table>
<thead>
<tr>
<th>Characteristic value</th>
<th>Lupa 1300-2</th>
<th>Lupa 3000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixels</td>
<td>1.3 MPixels</td>
<td>2.9 MPixels</td>
</tr>
<tr>
<td>Organization</td>
<td>1280 x 1024</td>
<td>1696 x 1710</td>
</tr>
<tr>
<td>Frame rate</td>
<td>500 fps</td>
<td>485 fps</td>
</tr>
<tr>
<td>Pixel size</td>
<td>14 x 14 μm²</td>
<td>8 x 8 μm²</td>
</tr>
<tr>
<td>Image area</td>
<td>17.9 x 14.3 mm²</td>
<td>13.6 x 13.7 mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>CMOS 0.25 μm</td>
<td>CMOS 0.25 μm</td>
</tr>
<tr>
<td>Analog/digital converter</td>
<td>10 bit</td>
<td>8 bit</td>
</tr>
<tr>
<td>SNR</td>
<td>58 dB</td>
<td></td>
</tr>
<tr>
<td>Output channels</td>
<td>12 (LVDS)</td>
<td>32 (LVDS)</td>
</tr>
<tr>
<td>Output frequency</td>
<td>310 MHz (DDR)</td>
<td>206 MHz (DDR)</td>
</tr>
<tr>
<td>Throughput</td>
<td>13.3 Gbit/s</td>
<td></td>
</tr>
<tr>
<td>Image throughput</td>
<td>1.4 GPixel/s</td>
<td></td>
</tr>
<tr>
<td>Additional functions</td>
<td>FPN correction</td>
<td>Microlenses</td>
</tr>
<tr>
<td></td>
<td>Multiple slope</td>
<td></td>
</tr>
<tr>
<td>Verlustleistung</td>
<td>1.1 W</td>
<td>1.1 W</td>
</tr>
</tbody>
</table>

**INFO: Overview of operating modes**

*With the correlated double sampling* in rolling shutter mode, the RESET signal is stored at the beginning of the exposure time and read together with the signal at the end of the exposure time. This eliminates both FPN (Fixed Pattern Noise) and kT/C noise.

*With double sampling* in snapshot shutter mode, the pixel signal is stored at the end of the exposure time and the RESET signal is generated during readout. This cancels out the FPN but not the kT/C noise, because the signal and RESET values originate from different RESET operations.

*Finally, in pipelined snapshot shutter mode*, only the pixel signal is output at the end of the integration time, and the RESET signal is ignored. This mode ensures maximum data throughput, as the current frame is integrated while the previous frame is still being read. A drawback of using a 6T pixel in this operating mode is that there is no on-chip FPN correction. But when maximum throughput is required, there is no alternative to pipelined snapshot shutter mode. In this mode, however, the parasitic light sensitivity (PLS) must be observed, which expresses the influence of the current image on the previous image which is still being read out. This influence should be as low as possible. Fortunately, the 6T pixel performs better here than a 5T buried diode pixel that can also be used in pipelined snapshot shutter mode: Thus the PLS of the pixel structure employed in both sensors is better than 1:4000. The disadvantage of this fast mode is a slight increase in the noise level, but this is not critical for most applications. Finally, in the smaller sensor a 14 μm pixel pitch ensures very high sensitivity, while the only 8 μm pixels of the higher-resolution sensor are equipped with microlenses for optimum quantum efficiency and fill factor. Both sensors also have a high conversion gain, which minimizes the required integration time.
of the individual data links. But this by-
no-means trivial measure is supported by
the sensor, which, in training mode, sends
a known training pattern over each data
channel to facilitate the calibration in the
host system.

The synchronization channel transports
start-of-frame, end-of-frame, start-of line
and end-of-line information as well as the
current line number. To allow error detec-
tion at the receive end, the sensor com-
cipulates each transmitted line with a cyclic
redundancy check (CRC) word.

The transmission channels are equipped
with parameterizable drivers which com-
ply with the LVDS standards ANSI/TIA/
EIA-644-A-2001. They consist of a pro-
grammable current sink which defines the
drive current, a dynamically controlled
current source, a 4-transistor bridge which
steers these currents to the differential
outputs, and a common-mode feedback
circuit to balance the sink and source cur-
rents.

**Summary: Autonomous sensor for flexible cameras**

These off-the-shelf, immediately usable CMOS image sensors provide a
largely autonomous and easy-to-install functional unit, which allows flexible
camera concepts with superior perform-
ance data to be implemented more
quickly and cost-effectively than was
previously possible with customized
sensors. This advancement is set to fa-
cilitate and accelerate the development
of new fields of application for optical
inspection and process control.

**AUTOR**

PIETER WILLEMS is Sr. Staff Applications Engineer with
Cypress Semiconductor in Mechelen/Belgien.